CLAIMS

What is claimed is:

1. A frame processing unit for transmitting data frames of varying priorities on a network medium comprising:

a) a frame buffer management circuit receiving data frames and storing data frames in a buffer memory;

b) a register storing data representing the existence of data frames of a designated priority in the buffer memory;

c) a priority resolution circuit, reading the register to determine the highest priority data frame available for transmission; and

d) a frame transmission circuit receiving an address of the highest priority data frame from the priority resolution circuit, receiving a signal from a media access controller indicating that a frame may be transmitted, retrieving a frame from the buffer memory corresponding to the address, and making the data frame available to the media access controller for transmitting to the network medium.

2. The frame processing unit of claim 1, wherein priority resolution circuit continually retrieves data from the register to determine highest priority data frame in the buffer memory and replaces an address previously provided to the frame transmission circuit if a higher priority frame becomes available.

3. The frame processing unit of claim 2, wherein the frame buffer is a random access memory frame buffer.

4. The frame processing unit of claim 3, further including a random access memory pointer table storing an indicator of the priority for each frame in the frame buffer along with the address location of each frame in the fame buffer.

5. The frame processing unit of claim 4, wherein the frame buffer management circuit locates the address of the highest priority frame, as indicated by the register, from the random access memory pointer table.

6. The frame processing unit of claim 5, wherein the media access controller receives the frame from the frame transmission circuit and makes each frame available to physical layer circuitry.

7. The frame processing unit of claim 6, wherein the frame transmission frame circuit, upon transmission of a frame to the media access controller, sends a command to the priority resolution circuit which in turn updates the register and the random access memory pointer table to reflect transmission of the frame.

8. The frame processing unit of claim 7, wherein the frame buffer management circuit receives and stores data frames from an application via a peripheral bus.

9. The frame processing unit of claim 8, wherein data received via the peripheral bus may include data of varying priorities as assigned by the application.

10. A method of transmitting the highest priority data frame available in a frame buffer, the method comprising:

a) reading data from a register to determine the priority of the highest priority data frame available for transmission;

b) locating a frame buffer address at which the highest priority frame is stored in a frame buffer;

c) writing the address of the highest priority data frame to a frame transmission circuit;

d) overwriting the address of the highest priority data frame with the address of a new highest priority data frame if a new higher yet priority data frame becomes available; and

e) retrieving the new highest priority data frame from the frame buffer and transmitting the new highest priority data frame when the network media is available.

11. The method of claim 10, further including updating the register upon transmission of a data frame to reflect transmission of the data frame.

12. The method of claim 11, wherein the step of locating the frame buffer address includes looking up the frame buffer address in a pointer table which stores the frame buffer address along with the priority of the frame stored at the address.

13. The method of claim 12, further including updating the pointer table upon transmission of a data frame to reflect transmission of the data frame.

14. A network computer comprising:

a) a central processing unit operating a plurality of applications generating data frames of varying priorities for transmission on a network medium;

b) a network interface circuit receiving the data frames and transmitting the data frames on the network medium in priority order, the network interface circuit including:

i) a frame buffer management circuit receiving data frames from the central processing unit and storing data frames in a buffer memory;

ii) a register storing data representing the existence of data frames of a designated priority in the buffer memory;

iii) a priority resolution circuit, reading the register to determine the highest priority data frame available for transmission; and

iii) a frame transmission circuit receiving an address of the highest priority data frame from the priority resolution circuit, receiving a signal from a media access controller indicating that a frame may be transmitted, retrieving a frame from the buffer memory corresponding to the address, and making the

data frame available to the media access controller for transmitting to the network medium.

15. The network computer of claim 14, wherein priority resolution circuit continually retrieves data from the register to determine highest priority data frame in the buffer memory and replaces an address previously provided to the frame transmission circuit if a higher priority frame becomes available.

16. The network computer of claim 15, wherein the frame buffer is a random access memory frame buffer.

17. The network computer of claim 16, further including a random access memory pointer table storing an indicator of the priority for each frame in the frame buffer along with the address location of each frame in the fame buffer.

18. The network computer of claim 17, wherein the frame buffer management circuit locates the address of the highest priority frame, as indicated by the register, from the random access memory pointer table.

19. The network computer of claim 18, wherein the media access controller receives the frame from the frame transmission circuit and makes each frame available to physical layer circuitry.

20. The network computer of claim 19, wherein the frame transmission frame circuit, upon transmission of a frame to the media access controller, sends a command to the priority resolution circuit which in turn updates the register and the random access memory pointer table to reflect transmission of the frame.

21. The network computer of claim 20, wherein the frame buffer management circuit receives and stores data frames from an application via a peripheral bus.

22. The network computer of claim 21, wherein data received via the peripheral bus may include data of varying priorities as assigned by the application.

23. The network computer of claim 22, wherein the frame buffer management circuit includes a random access memory frame buffer to store the data frame.